



ABSTRACT OF THE DISCLOSURE

The data sharing apparatus in the present invention includes a first processor and a second processor, each of a different endianness, that are both connected to the memory via the data bus, in a byte order based on
5 the endianness of the first processor. It also includes an address conversion unit which converts at least one lower bit of an address to indicate a reversed position of data in the data bus, and outputs the converted address to the memory, in the case where the second processor performs a memory access on the shared memory for data with a smaller
10 width than the data bus.